CLAIM AMENDMENTS

Claims 1-4 (Cancelled).

5. (Currently Amended) The real-time stereo image matching system of claim ~~4~~ 17, wherein the system includes N processing means, N/2 first storage means, and N/2 second storage means where N is an integer multiple of 2.

6. (Original) The real-time stereo image matching system of claim 5, wherein the processing means exchanges information with neighboring processing means.

7. (Currently Amended) The real-time stereo image matching system of claim 5, wherein, among the N processing means, only a processing means that outputs ~~the~~ a predetermined disparity is activated at one time and the remaining processing means are in high impedance states.

Claims 8-11 (Cancelled).

12. (Currently Amended) The real-time stereo image matching system of claim ~~11~~ 19, wherein, when a write control signal is input from outside, the ~~first~~ forward processor operates, and when a read control signal is input from outside, the ~~second~~ backward processor operates.

13. (Currently Amended) The real-time stereo image matching system of claim ~~11~~ 19, wherein the decision storage means has a last-in first-out structure in which the decision value that is output last from the ~~first~~ forward processor is first input to the ~~second~~ backward processor.

14. (Currently Amended) The real-time stereo image matching system of claim ~~11~~ 19, wherein the first processor comprises:

matching cost calculating means for calculating a matching cost, using a pixel of one line of a digital image stored in the first storage means and the second storage means;

first adding means for adding the calculated matching cost to ~~the fed back~~ an accumulated cost;

comparing means for comparing the output of the first adding means with the costs of neighboring processing means, and then outputting the minimum matches of cost and decision value;

storage means for storing the minimum cost that is a comparison produced by the comparison means, as the accumulated cost; and

second adding means for adding ~~the~~ an entire cost and an occlusion cost to produce a sum, and then outputting the sum to neighboring processing means.

15. (Currently Amended) The real-time stereo image matching system of claim ~~11~~ 14, wherein the ~~second~~ backward processor comprises:

logical OR means for OR-ing activation information of the neighboring processing means and feed-back activation information route;

a register for storing the last activation information produced by the logical OR means;

demultiplexing means for demultiplexing the last activation information according to the decision value output from the decision storage means and outputting to the neighboring processing means and feeding back to the logical OR means; and

a tri-state buffer for outputting the decision value output from the decision storage means, as a determined disparity, according to the activation information of the register.

16. (Currently Amended) The real-time stereo image matching system of claim ~~17~~ 15, wherein the output from the decision storage means controls which direction the demultiplexing means passes the activation information.

17. (New) A real-time stereo-matching system comprising:

first and second cameras having respective parallel optical axes and co-planar focal planes;

signal converting means for converting an image input from the first camera and an image input from the second camera into respective digital signals;

first storage means for storing pixels of the digital image from the first camera;

second storage means for storing pixels of the digital image from the second camera;

processing means including a plurality of even-numbered processors and a plurality of odd-numbered processors, for outputting an estimated disparity using pixels input from the first and second storage means; and

clock control means for outputting a first clock signal provided to the even-numbered processors of the processing means and to the second storage means, and a second clock signal provided to the odd-numbered processors of the processing means and the first storage means, to control operation of the first and second storage means and the processing means.

18. (New) A real-time stereo-matching system comprising:

first and second cameras having respective parallel optical axes and co-planar focal planes;

signal converting means for converting an image input from the first camera and an image input from the second camera into respective digital signals;

first storage means for storing pixels of the digital image from the first camera;

second storage means for storing pixels of the digital image from the second camera;

processing means for outputting an estimated disparity using pixels input from the first and second storage means; and

clock control means for outputting a clock signal for controlling operation of the first and second storage means and the processing means, wherein the first storage means and the second storage means are initialized when the processing means completes processing of pixels in one scan line.

19. (New) A real-time stereo-matching system comprising:

first and second cameras having respective parallel optical axes and co-planar focal planes;

signal converting means for converting an image input from the first camera and an image input from the second camera into respective digital signals;

first storage means for storing pixels of the digital image from the first camera;

second storage means for storing pixels of the digital image from the second camera;

a forward processor receiving a pixel of one scan line of the digital images in the first and second storage means and outputting a matching cost and decision value;

decision storage means for storing the decision value output by the forward processor;

a backward processor for outputting an estimated disparity, using decision values output from the decision storage means, in response to activation information; and

clock control means outputting a clock signal for controlling operation of the first and second storage means and the forward and backward processors.